

# **JEDEC PERFORMANCE STANDARD**

## **CONNECTOR PERFORMANCE STANDARDS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS**

### **JEDEC PUBLICATION 95**

#### **PS-001A**

#### **240 Pin DDR3**

#### **(Double Data Rate 3, UDIMM)**

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**JEDEC  
SOLID STATE TECHNOLOGY ASSOCIATION**

**Date: OCTOBER 2007  
Item: 11.14-109(S)**

**Issue: A**

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## 240 Pin DDR3 UDIMM Performance Standard

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## 240 pin DDR3 UDIMM Performance Standard

### 1 Scope

The purpose of this document is to ensure form, fit, and function of the DDR3 connector. It contains the connector Mechanical and Electrical specifications and requirements. This document supersedes all other Intel DDR3 connector related documents.

NOTE S-parameter electrical specifications governed by JC45.5 document.

### 2 Reference documents

Document #	Document	Published date
MO-269B	JEDEC Document: MO (Module Outline)	May 2006
SO-007A	JEDEC Document: SO (Socket Outline)	July 2006
EIA-364D	Electrical Connector/Socket Test Procedures Including Environmental Classifications	July 2001
EIA-364-1000.01	Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Business Office Applications	January 2001
JESD22-B-102D	JEDEC Document: Solderability	September 2004
Intel Raptor 3C	DDR3 Connector High Speed Electrical Test Procedure document	
GS-005A	Insertion, Extraction Force Gauge	July 2006

### 3 Connector pinout

Pin #			Pin #
1	Pin	Pin	121
2	Pin	Pin	122
3	Pin	Pin	123
4	Pin	Pin	124
5	Pin	Pin	125
6	Pin	Pin	126
7	Pin	Pin	127
8	Pin	Pin	128
9	Pin	Pin	129
10	Pin	Pin	130
11	Pin	Pin	131
12	Pin	Pin	132
13	Pin	Pin	133
14	Pin	Pin	134
15	Pin	Pin	135
16	Pin	Pin	136
17	Pin	Pin	137
18	Pin	Pin	138
19	Pin	Pin	139
20	Pin	Pin	140
21	Pin	Pin	141
22	Pin	Pin	142
23	Pin	Pin	143
24	Pin	Pin	144
25	Pin	Pin	145
26	Pin	Pin	146
27	Pin	Pin	147
28	Pin	Pin	148
29	Pin	Pin	149
30	Pin	Pin	150
31	Pin	Pin	151
32	Pin	Pin	152
33	Pin	Pin	153
34	Pin	Pin	154
35	Pin	Pin	155
36	Pin	Pin	156
37	Pin	Pin	157
38	Pin	Pin	158
39	Pin	Pin	159
40	Pin	Pin	160

Pin #			Pin #
41	Pin	Pin	161
42	Pin	Pin	162
43	Pin	Pin	163
44	Pin	Pin	164
45	Pin	Pin	165
46	Pin	Pin	166
47	Pin	Pin	167
48	Pin	Pin	168
Key Key Key Key			
49	Pin	Pin	169
50	Pin	Pin	170
51	Pin	Pin	171
52	Pin	Pin	172
53	Pin	Pin	173
54	Pin	Pin	174
55	Pin	Pin	175
56	Pin	Pin	176
57	Pin	Pin	177
58	Pin	Pin	178
59	Pin	Pin	179
60	Pin	Pin	180
61	Pin	Pin	181
62	Pin	Pin	182
63	Pin	Pin	183
64	Pin	Pin	184
65	Pin	Pin	185
66	Pin	Pin	186
67	Pin	Pin	187
68	Pin	Pin	188
69	Pin	Pin	189
70	Pin	Pin	190
71	Pin	Pin	191
72	Pin	Pin	192
73	Pin	Pin	193
74	Pin	Pin	194
75	Pin	Pin	195
76	Pin	Pin	196
77	Pin	Pin	197
78	Pin	Pin	198
79	Pin	Pin	199
80	Pin	Pin	200

Pin #			Pin #
81	Pin	Pin	201
82	Pin	Pin	202
83	Pin	Pin	203
84	Pin	Pin	204
85	Pin	Pin	205
86	Pin	Pin	206
87	Pin	Pin	207
88	Pin	Pin	208
89	Pin	Pin	209
90	Pin	Pin	210
91	Pin	Pin	211
92	Pin	Pin	212
93	Pin	Pin	213
94	Pin	Pin	214
95	Pin	Pin	215
96	Pin	Pin	216
97	Pin	Pin	217
98	Pin	Pin	218
99	Pin	Pin	219
100	Pin	Pin	220
101	Pin	Pin	221
102	Pin	Pin	222
103	Pin	Pin	223
104	Pin	Pin	224
105	Pin	Pin	225
106	Pin	Pin	226
107	Pin	Pin	227
108	Pin	Pin	228
109	Pin	Pin	229
110	Pin	Pin	230
111	Pin	Pin	231
112	Pin	Pin	232
113	Pin	Pin	233
114	Pin	Pin	234
115	Pin	Pin	235
116	Pin	Pin	236
117	Pin	Pin	237
118	Pin	Pin	238
119	Pin	Pin	239
120	Pin	Pin	240

## 4 Mechanical drawings

### 4.1 Connector footprint

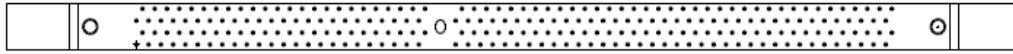


Figure 4.1.1 — PCB Connector Footprint refer to JEDEC SO-007 for details

### 4.2 Connector outline

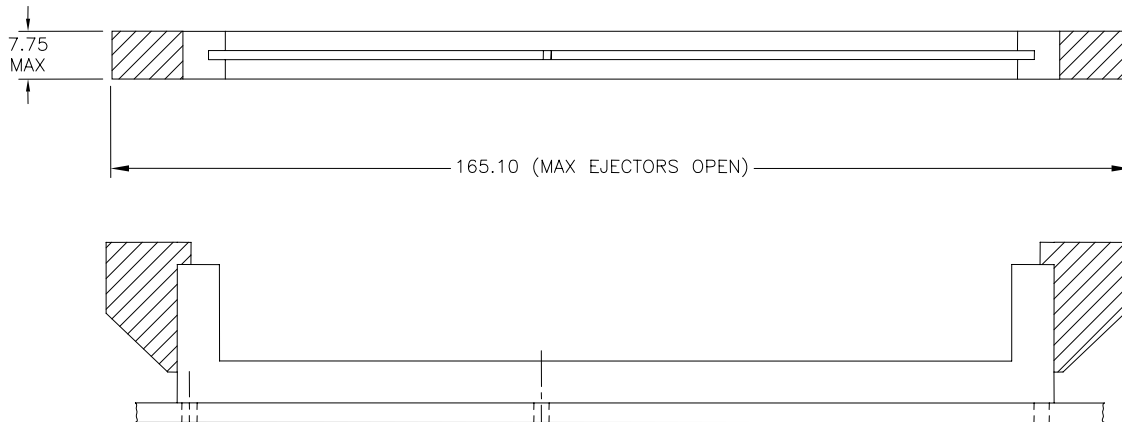


Figure 4.2.1 — Connector Outline refer to JEDEC SO-007 for details

### 4.3 Module outline

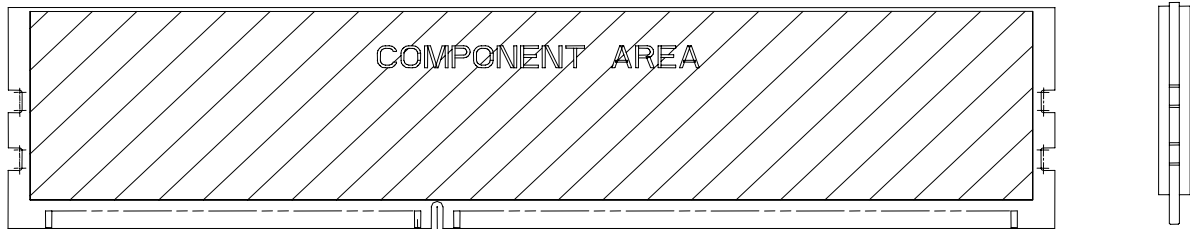


Figure 4.3.1 — Module Profile, refer to JEDEC MO-269 for details



## 5 Connector requirements

Use EIA-364 and EIA-TS-1000 to determine test sequence and sample size unless specified.

### 5.1 Mechanical requirements

Specification	"Pass" criteria	Measurement procedure
Visual and dimensional inspections.	Meets product drawing	Gauge accuracy shall be 10 times more accurate than tolerance specified on drawing and be traceable to NIST.
Insertion Force (Module to Connector)	106.8 N	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min. Use the JEDEC GS-005 module thickness gauge.
Retention Force - Terminal	300gf min per pin; no movement of contact more than 0.38 mm	EIA 364-29
Retention Force - Forklock	13.3 N min per forklock; max movement of 0.38 mm	EIA 364-29
Insertion Force - Connector to Board	75 N maximum.	EIA-364-05 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 2.7 mm/min; GS-008 gauge.
Unmating Force (per pin pair)	14 gf min.	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 12.7 mm/min GS-005 Gauge

### 5.2 AC electrical requirements

Specification	"Pass" criteria	Measurement procedure
L11 (signal loop inductance)	2.5 to 3.5 nH @ 266, 333, and 400 MHz	See 6.4 and Annex A.
C11 (coupling capacitance between adjacent signals)	0.3 to 0.6 pF @ 266, 333, and 400 MHz	See 6.4 and Annex A.
L12 (Mutual inductance between adjacent signals)	0.9 nH Max @ 266, 333, and 400 MHz	See 6.4 and Annex A.
C12 (mutual capacitance between adjacent signals)	0.3 pF Max @ 266, 333, and 400 MHz	See 6.4 and Annex A.

## 5 Connector requirements (cont'd)

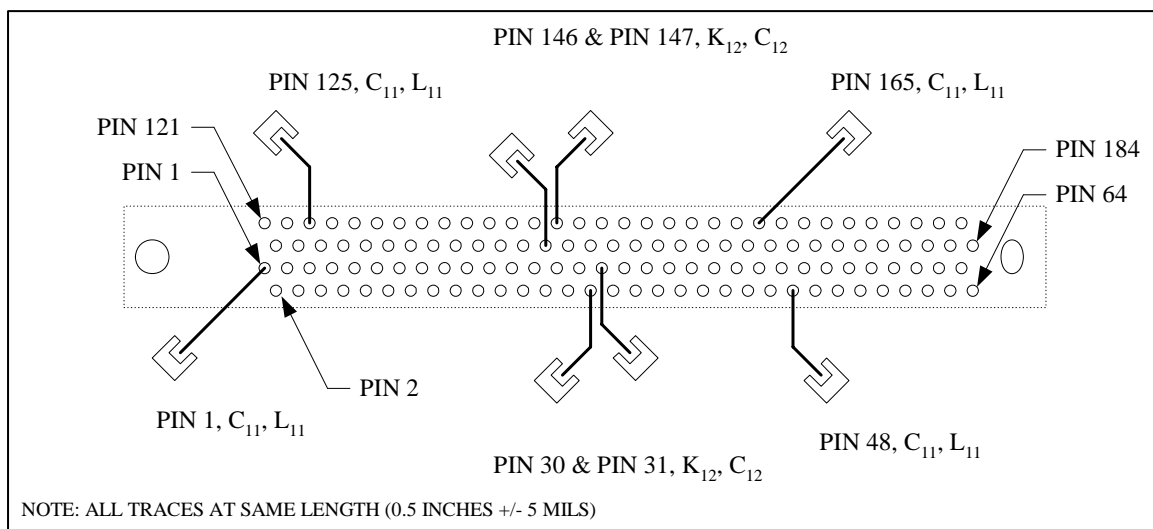
### 5.3 DC electrical requirements

Specification	"Pass" Criteria	Measurement Procedure
Contact resistance, initial	30 mΩ Max	EIA-364 -23
Current carrying capability at 30 °C temperature rise per contact	0.5 amp/pin De-rated	EIA-364 Test Procedure 70. Ten pairs contacts in consecutive positions (pins 65-74 and pins 185-194) on the same side of the connector are connected in a series circuit (mated condition). A thermocouple is inserted though holes in the socket housing, as close to the contact interface as possible. Supply 0.5 A current; temperature rise shall not exceed 30 °C
Withstand Voltage	500 v	EIA-364-20
Insulation resistance	1 MΩ Min	EIA-364-21

### 5.4 AC electrical measurements

Figure 5.4.1 illustrates signal test points for electrical measurements defined in this section. Measurements shall be taken at three frequencies: 266, 333 and 400 MHz, using a Vector Network Analyzer (VNA). For maximum accuracy, the trace length between the signal launch point and the DDR3 connector should be minimized, and the trace impedance defined as 50 ( $\pm 10\%$ )  $\Omega$ . Refer to Annex A for details on the DUT board and DUT module.

NOTE Shown are DDR2 DUT test board and module. Methodology is same for DDR3 measurements.



**Figure 5.4.1 — 240 pin test board footprint illustration\***

\* Figure only shows the Left half of the footprint. All measurements must be made at room temperature and humidity conditions, not to exceed 65% RH (non-condensing).

## **5.4 AC electrical measurements (cont'd)**

### **5.4.1 Loop inductance**

Using the VNA, loop inductance is measured by launch of a signal onto a signal pin short-circuited to its neighboring ground pin. The contribution due to the test board must be calibrated out. Refer to Annex A for detailed procedures.

### **5.4.2 Capacitance**

Using the VNA, total loading capacitance of a pin is measured by launch of a signal onto a signal pin that is open-circuited. The contribution due to the test board must be calibrated out. Refer to Annex A for detailed procedures.

### **5.4.3 Coupling coefficients**

The mutual inductance and capacitance are measured by a 2-port measurement using the VNA. Refer to Annex A for detailed procedures.

## **5.5 Environmental requirements**

Follow EIA 364-1000.01 for environmental tests, using:

- Durability (mating/unmating) rating of 25 cycles: GS-005 maximum insertion force gauge
- Temperature life test temperature and duration: for 3, 5, and 7 year life per EIA 364-1000
- Temperature life test temperature and duration for preconditioning: for 3, 5, and 7 year life per EIA-364-1000
- Mixed flowing gas test duration: Test using for 3, 5, and 7 year life per EIA-364-1000
- Maximum allowable LLCR change (between reading after testing and the initial reading: 20 m $\Omega$ )

## 5.5 Environmental requirements (cont'd)

Replace the Test Group 3 in EIA-364-1000 with:

Specification & Test Sequence	"Pass" Criteria	Measurement Procedure	Condition of test specimens
1. Low level contact resistance	30 mΩ max (initial)	EIA-364-23 (Termination of connector to base board and add-in card shall be included in measurements)	Mated
2. Preconditioning	No evidence of physical damage	EIA-364-09 Perform 5 plug/unplug cycles.	
3. Low level contact resistance	20 mΩ max resistance increase	EIA-364-23 (Termination of connector to base board and add-in card shall be included in measurements)	Mated
4. Random Vibration	No discontinuities of 1 microsecond or longer duration.  No evidence of physical damage	EIA-364-28 Subject 4 continuity and 4 termination resistance specimens to input acceleration 3.13 g RMS between 5 Hz to 500 Hz, 10 minutes per axis to: 5 to 20Hz (slope): (0.01g <sup>2</sup> /Hz)@5Hz, (0.02g <sup>2</sup> /Hz)@20Hz; 20 to 500Hz (flat): (0.02g <sup>2</sup> /Hz)@20Hz; Random control limit tolerance: ± 3 dB. Module weight 35g +/- 5g with the center of gravity of 20-25 mm from the module mating edge. Duration: 10 minutes per axis for all 3 axes on all samples. Test board defined in Figure 5.5.1.	Mated
5. Low level contact resistance	20 mΩ max resistance increase over the initial	EIA-364-23 (Termination of connector to base board and add-in card shall be included in measurements)	Mated
6. Physical shock	No discontinuities of 1 microsecond or longer duration.  No evidence of physical damage	EIA-364-27 Subject 4 continuity and 4 termination resistance specimens to input acceleration 3.13 g RMS between 5 Hz to 500 Hz, 10 minutes per axis to: Profile: Trapezoidal shock of 50 g. ± 10% Duration: 11 ms Minimum Velocity change: 67 cm/sec, ± 10%. Module weight 35g +/- 5g with the center of gravity of 20-25 mm from the module mating edge. Quantity: Three drops in each of six directions, applied to three sample boards. Test board defined in Figure 5.5.1	Mated
7. Low level contact resistance	20 mΩ max resistance increase over the initial	EIA-364-23 (termination of connector to base board and add-in card shall be included in measurements)	Mated

## 5.5 Environmental requirements (cont'd)

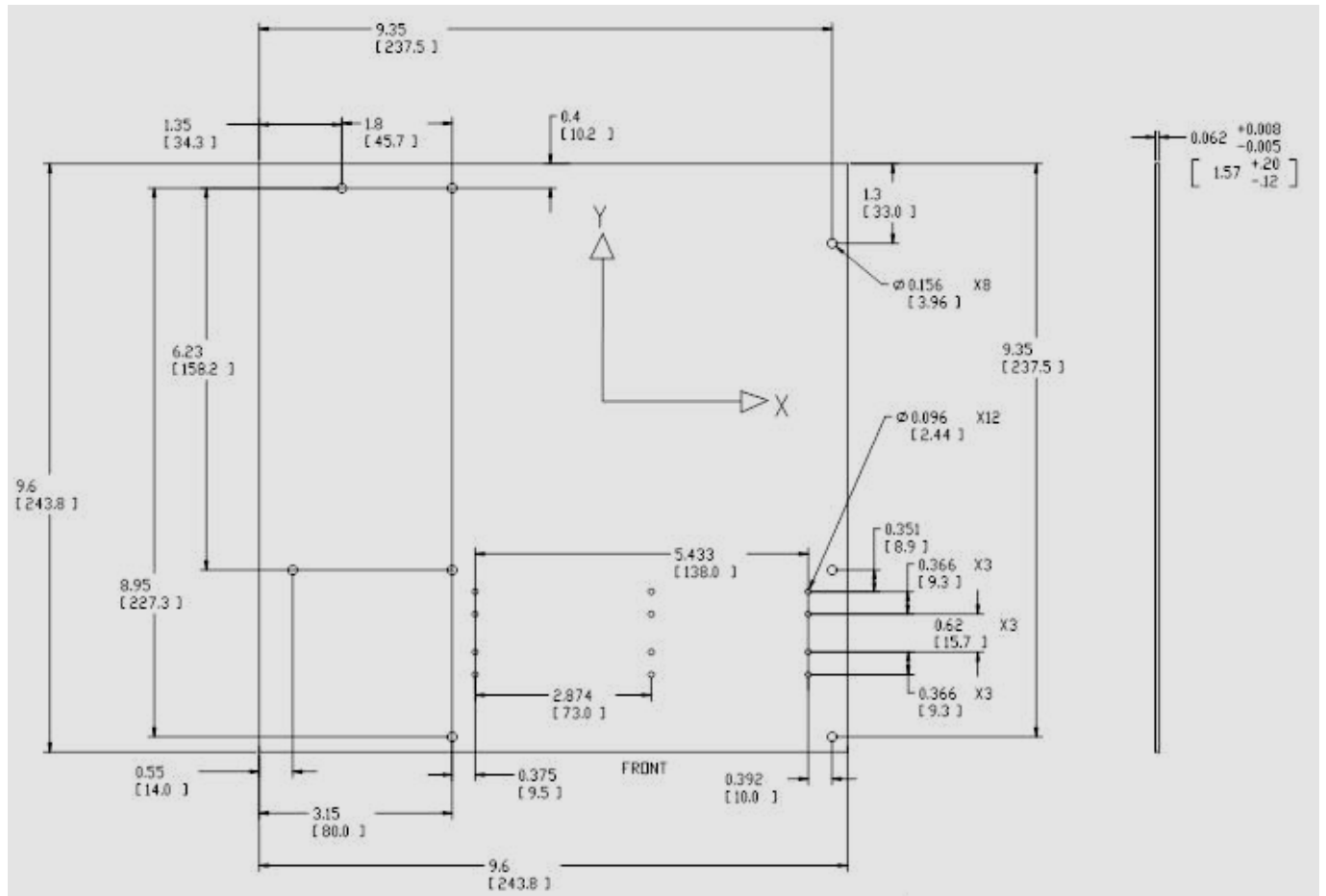


Figure 5.5.1 — System level shock and vibration test fixture, micro ATX

## 5.6 Other requirements

Specification	“Pass” Criteria	Measurement Procedure
Material	UL94 V0	UL 94-V0. Material Certification or certificate of compliance to UL service requirements
Solderability - Lead Free	95% coverage	JESD22-B102; Condition C, 8 hours ± 15 minutes steam precondition.
Lead Free Process ability	No physical damage to connector per visual inspection at 24 inches. No magnification	260 °C, 5 seconds.

## Annex A Measurement of connector parasitics

### A.1 Required equipment

Vector Network Analyzer (VNA).

Microprobes - The choice to be made is based on package pitch and signal-ground orientation of the test fixture. Recommend 1000  $\mu\text{m}$  pitch probes for 0.5-1.0 mm pin pitch devices. Correct calibration standard for the probe type must be used.

Calibration Standard - Microprobe calibration standards can be purchased from probe suppliers.

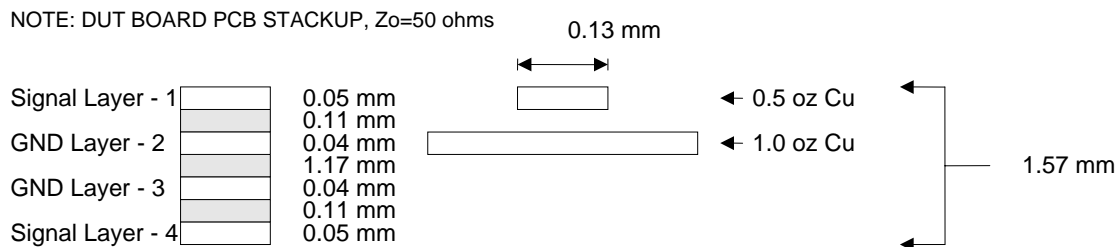
The calibration standard is a high precision ceramic substrate that provides open, short, thru, and 50  $\Omega$  loads that can be used to calibrate out the effects of cables and probes.

Two 50  $\Omega$  high frequency, low loss phase-matched cables. The cables are used to connect the microprobes to the measurement ports on the VNA.

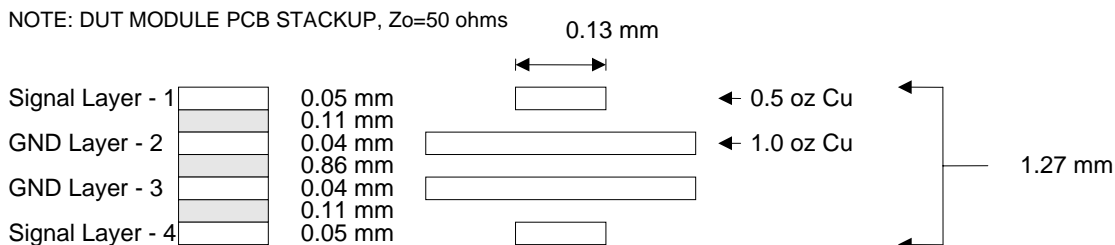
### A.2 Test fixture and samples

Figure A.1 and Figure A.2 describe details of the 4-layer DUT board and DUT module PCB stackup to be used. Reference designs to include PCB stackup and specifications of the DUT module card can be provided to connector manufactures per request. The DUT board and DUT module impedance are defined as 50 ( $\pm 10\%$ ) ohms.

NOTE Shown are DDR2 DUT test board and module. Methodology is same for DDR3 measurements.



**Figure A.1 – DUT board PCB stackup**

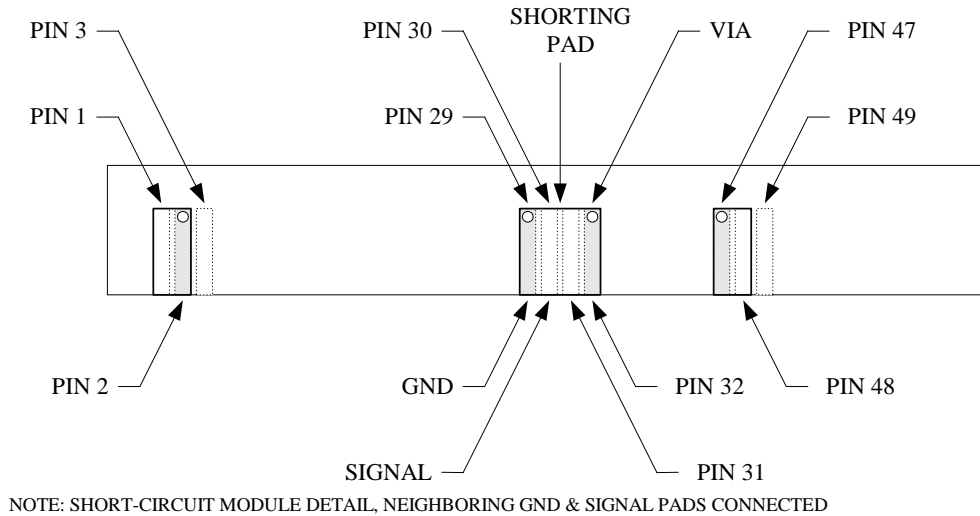


**Figure A.2 — DUT module PCB stackup**

NOTE This diagram is intended as an example only. Each manufacturer can determine the thickness of their layers based on the own impedance calculations.

## A.2 Test fixture and samples (cont'd)

Figure A.3 describes details of the 4-layer DUT module to be used. Reference designs to include PCB stackup and specifications of the DUT module card can be provided to connector manufactures per request. The DUT module is a printed circuit board with shorting pads. The thickness of the module is 1.27 mm.



**Figure A.3 — Short-circuit module card**

## A.3 Sample preparation

DUT board and DUT module shall be for electrical test only. Align the connector pins with the corresponding through holes vias of the DUT board. Firmly press the connector into the board with uniform pressure across the connector body until all of the connector standoff points are flush with the DUT board surface. Use wave solder process to mate the connector and DUT board. Ensure that the gap between the DUT board and the connector standoff must be less than 0.05 mm to be considered a good sample.

## A.4 Network analyzer calibration

For all measurements, the DUT fixture must be calibrated so that device measurements do not include fixture inductance and capacitance parasitics of cables, probes, and the DUT board. These parasitic parameters need to be nulled out of the measured data. Obtain the calibration data of the probes from the supplier and enter the data into the "Calibration Kit" before performing the calibration.

A full two-port calibration is required before the measurement. The following is a systematic procedure for vector network analyzer and microprobe calibration.

Frequency	:	100 MHz-1000 MHz
Number of Points	:	801
Number of Averages	:	32
IF BW	:	300Hz
Cal	:	Full 2-Port
L/C	:	266 MHz, 333 MHz, and 400 MHz
Mutual	:	266 MHz, 333 MHz, and 400 MHz

NOTE (HK) = HardKey Menu Option, and (SK) = SoftKey Menu Option



#### A.4 Network analyzer calibration (cont'd)

Full 2-port slot Calibration Procedure:

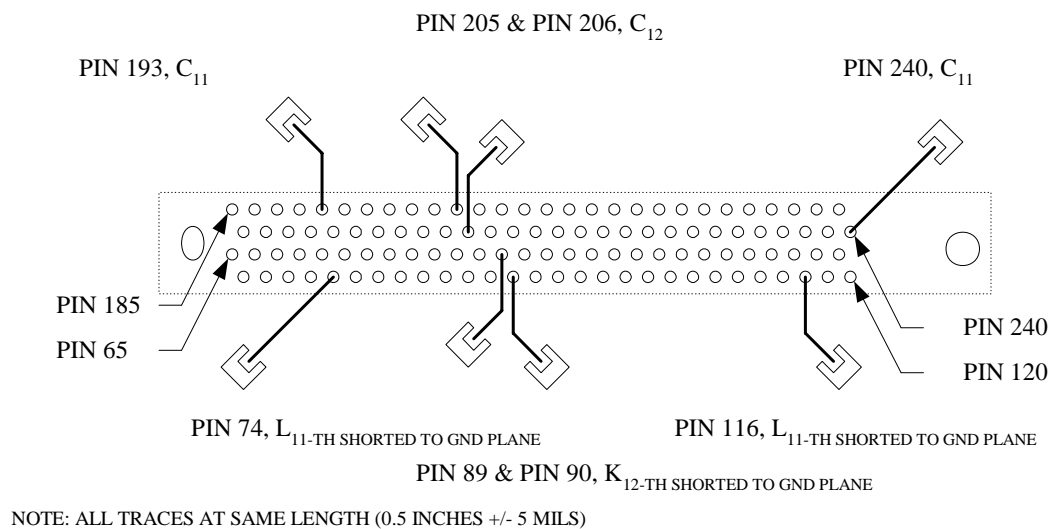
- Set Start/Stop Frequency
  - (HK) Start
  - (HK) 100 M/u (100 MHz)
  - (HK) Stop
  - (HK) 1 G/u (1 GHz)
- Number of Points
  - (HK) Sweep Setup
  - (SK) Number of Points (801)
- Turn on Averaging and set number of averages
  - (HK) Avg
  - (SK) Averaging (ON)
  - (SK) Averaging Factor (32 X1) (32 averages)
- Set IF bandwidth and system Z0
  - (SK) IF BW 300 X1 (300 Hz)
  - (SK) Smoothing (OFF)
- Set Impedance to 50
  - (HK) Cal
  - (SK) More
  - (SK) Set Z0 50 X1 (50 )
  - (SK) Return
- Turn on Interpolation, Correction is off
  - (HK) Cal
  - (SK) Interpolation ON
  - (SK) Correction OFF
- Select Cal Kit
  - (HK) Seq
  - (SK) More
  - (SK) Load Seq from Disk
  - (SK) Read Seq file Titles
  - (SK) Load Seq
- Press LOAD SEQ (overwrite existing sequence)
  - (HK) Seq
  - (SK) Do Seq
  - (SK) Sequence 1
  - (SK) Return
  - (HK) Cal
  - (SK) Cal Kit
  - (SK) Save User Kit
  - (SK) Select Cal Kit
  - (SK) User Kit
- Floppy Disk Save setup
  - (HK) Save/Recall
  - (SK) Select Disk
  - (SK) Internal Disk
  - (SK) Return
  - (SK) Define Disk Save
  - (SK) Data Array ON
  - (SK) Data Only ON
  - (SK) ASCII

## A.5 Measurement

In general, the capacitance measurement is performed using an open connector, while the inductance measurement is performed using a short-circuit test card.

### A.5.1 DUT board parasitics

Figure A.4 illustrates signal test points for electrical calibration measurements defined in this section. The contribution due to the DUT board must be calibrated out. The DUT board capacitance and inductance must be measured prior to the connector wave solder assembly to the DUT board. The DUT board  $C_{11}$  measurements are to be made with pin 193 and pin 240, and  $C_{12}$  measurements made with pins 205 and 206. The DUT board  $L_{11}$  measurements are to be made with pin 74 and pin 116, and  $K_{12}$  measurements made with pins 89 and 90.



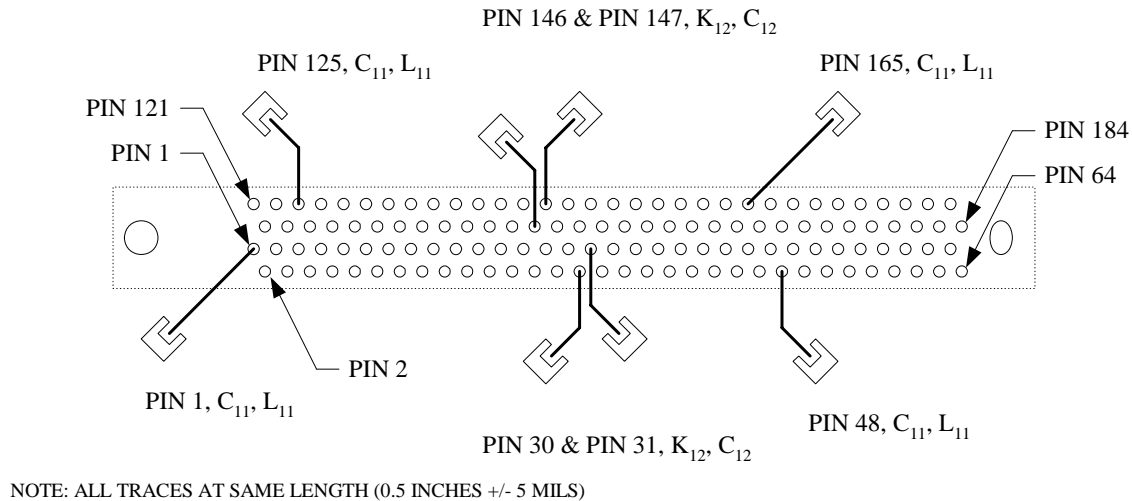
**Figure A.4 — 240 pin DUT board calibration structures\***

Using the capacitance calibration structure, 1-port s-parameter measurements of the DUT board  $C_{11}$  capacitance values can be read off the VNA at the required frequencies (266 MHz, 333 MHz, and 400 MHz) from the Smith chart format display. Using the inductance calibration structure, 1-port s-parameter measurements of the DUT board  $L_{11}$  inductance values can be read off the VNA at the required frequencies from the Smith chart format display.

Using the mutual capacitance calibration structure, a two-port s-parameter measurement of the DUT board  $C_{12}$  value can be read off the VNA at a required frequency, e.g., 400 MHz from the Smith chart format display. Using the mutual inductance calibration structure, a two-port s-parameter measurement of the DUT board  $L_{12}$  values can be read off the VNA at a required frequency, e.g., 400 MHz from the Smith chart format display.

\* Figure only shows the right half of the footprint

### A.5.2 Connector capacitance and inductance



**Figure A.5 — 240 Pin Test board footprint illustration\***

Figure A.5 illustrates signal test points for electrical measurements defined in this section. Measurements to be measured after the connector wave solder assembly to the DUT board must be subtracted from the calibration measurements to get the correct values.

To measure the capacitance, the open connector shall be used and pins 1, 48, 125, and 165 can be measured and averaged. A 1-port s-parameter measurement at a required frequency, say 400 MHz gives the capacitance value at the pin that is designated for capacitance measurement. This value is the total capacitance of the DUT board and the connector. The DUT board capacitance parasitic needs to be subtracted to get the connector capacitance, using averaged values from pin 193 and 240. Refer to Table A.1 in Section A.6.1 defining measurement procedures.

To measure the inductance, the short-circuit test module is inserted into the connector slot and pins 1, 48, 125, and 165 can be measured and averaged. A 1-port s-parameter measurement at a required frequency, say 400 MHz gives the inductance value at the pin that is designated for inductance measurement. This value is the total inductance of both the DUT board and the connector. The DUT board inductance parasitic needs to be subtracted to get the connector inductance, using averaged values from pin 74 and 116. The inductance value limits are applied to the average of two pin measurements of inductance. Refer to Table A.1.

Averaging for the inductance is used to compensate for soldering variation across the DUT board. If either individual pin measurement is greater than 0.8 nH from the two-pin average, the connector should be resoldered and the inductance retested.

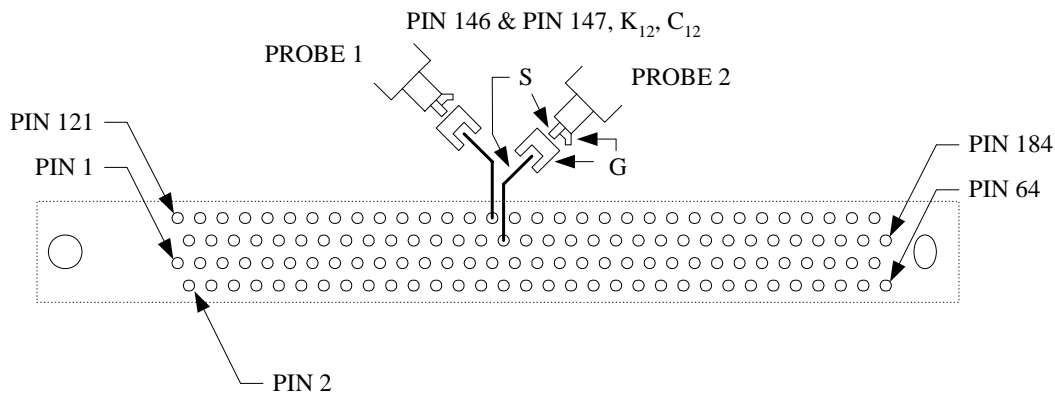
\* Figure only shows the left half of the footprint

### A.5.3 Mutual capacitance $C_{12}$

To measure the mutual capacitance, the open connector shall be used and pins 30 with 31 and pins 146 with 147 can be measured and averaged. Refer to Table A.1 in Section A.6.1 defining measurement procedures. The parameter of interest is the  $S_{12}$  coefficient. The DUT board mutual capacitance parasitic needs to be subtracted to get the connector capacitance, using values from pin 205 with 206. The mutual capacitance is given by

$$C_{12} = 1.59 \times 10^{-3} |S_{12}| / f \quad [1]$$

The slope of  $S_{12}(f)$  is taken from the low frequency range, and [1] is used to compute  $C_{12}$ . The measurement setup in Figure A6 is used.



NOTE: MICRO-PROBES USED.

**Figure A.6 — 240 Pin, Measure of mutual coefficients\***

### A.5.4 Mutual inductive coupling $L_{12}$

To measure the mutual inductance, the same measurement setup in Figure A.8 is used, except the short-circuit test module is inserted into the connector and pins 30 with 31 and pins 146 with 147 can be measured and averaged. Refer to Table A.1 in Section A.6.1 defining measurement procedures. The parameter of interest is the  $S_{12}$  coefficient. The DUT board mutual inductive coupling parasitic needs to be subtracted to get the connector mutual inductive coupling, using values from pin 89 with 90. The mutual inductive  $L_{12}$  is given by

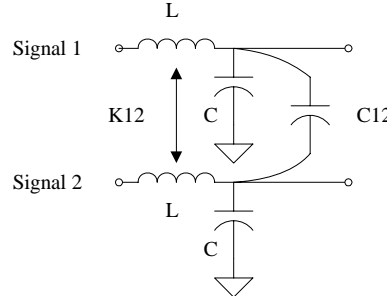
$$L_{12} = \frac{3.98 |S_{12}|}{f} \quad [2]$$

The slope of  $S_{12}(f)$  is taken from the low frequency range, and [2] is used to compute  $L_{12}$ .

\* Figure only shows the left half of the footprint

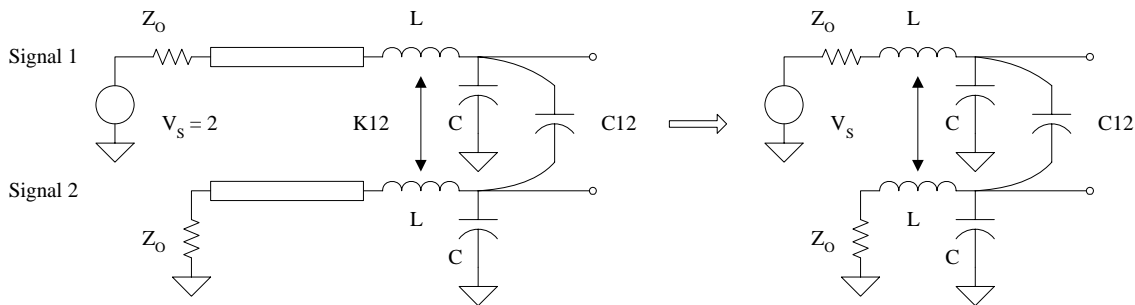
## A.6 Derivation of equations

Figure A.7 shows the equivalent circuit model of two signal pins including the effects of ground pins and ground plane(s).



**Figure A.7 — Equivalent circuit of two signal lines**

Figure A.8 shows the connector attached to a VNA under open-circuit condition. Since the signal line is open-circuited, to the first order, little current flows through the inductor and the effect of inductance can be ignored. The simplified circuit is shown on the right of Figure A.8.



**Figure A.8 — VNA measurement of two open signal lines**

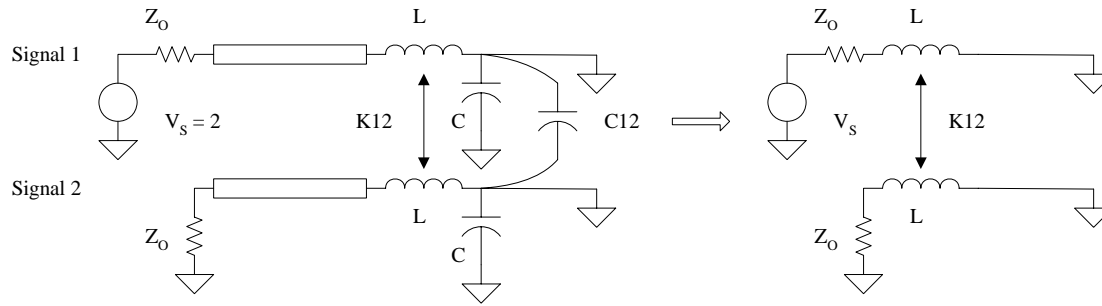
It can be derived that at low frequencies ( $1/j\omega C \gg Z_0$ ), the signal received by the second channel ( $S_{12}$ ) is given by

$$S_{12} \sim \frac{2Z_0 j\omega C_{12}}{1 + 2Z_0 j\omega C_{12}}$$

$$\sim 2Z_0 j\omega C_{12} = 4\pi Z_0 j f C_{12} \quad [3]$$

When the connector is measured under short-circuit condition, the circuit becomes as shown in Figure A.9. Since the signal line is short-circuited, to the first order, the voltage is small across the capacitors and only the inductors are considered. The simplified circuit is shown on the right of Figure A.9.

## A.6 Derivation of equations



**Figure A.9 — VNA measurement of two short signal lines**

Following analysis of the simplified circuit, it can be derived that the signal received by the second channel ( $S_{12}$ ) is given by

$$\begin{aligned}
 S_{12} &\sim \frac{2K_{12}j\omega L}{Z_0 + j\omega L} \\
 &\sim \frac{2K_{12}j\omega L}{Z_0} = \frac{4\pi L_{12}jf}{Z_0}
 \end{aligned}
 \tag{4}$$

## A.7 Report

Table A.1 shows a sample measurement table at 400 MHz. Similar tables can be made for other frequencies. Table is a sample of measurement summary table.

**Table A.1 — Sample measurement chart**

400 MHz	Calibration			DUT					Actual
	Pin 74	Pin 116	Avg1	Pin 1	Pin 48	Pin 125	Pin 165	Avg2	Avg2-Avg1
L11 (nH)									

400 MHz	Calibration			DUT					Actual
	Pin 193	Pin 240	Avg1	Pin 1	Pin 48	Pin 125	Pin 165	Avg2	Avg2-Avg1
C11 (pF)									

400 MHz	Calibration			DUT				Actual
	Pin 89/90			Pin 30/31		Pin 146/147		Avg
L12 (nH)								Avg-Cal

400 MHz	Calibration			DUT				Actual
	Pin 205/206			Pin 30/31		Pin 146/147		Avg
C12 (pF)								Avg-Cal

**Table A.2 — Sample qualification output**

Output Summary	266 MHz	333 MHz	400 MHz	Pass/Fail
L11				
C11				
L12				
C12				

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**Annex B (informative) Difference between revisions**

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Initial Issue: A	Date: October 2007	JC11 Item Number: 11.14-109
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<b>CHANGE RECORD HISTORY</b>
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Issue:	Date:	Item Number:
Description of changes		

Issue:	Date:	Item Number:
Description of changes		

Issue:	Date:	Item Number:
Description of changes		



